## REMARKS

In the June 9, 2003 Office Action, the Examiner noted that claims 1-17 were pending in the application; rejected claims 1-3, 5, 6, 8-10, 12-15 and 17 under 35 U.S.C. § 102(b); and rejected claims 4, 7, 11 and 16 under 35 U.S.C. § 103. In rejecting the claims, U.S. Patents 5,142,630 to Ishikawa; 4,881,170 to Morisada; and 5,963,721 to Shiell et al. (References A-C, respectively) were cited. Claims 1-17 remain in the case. The Examiner's rejections are traversed below.

### Rejections under 35 U.S.C. §§ 102(b) and 103

In paragraphs 3-16 on pages 2-6 of the Office Action, the Examiner rejected claim 1-3, 5, 6, 8-10, 12-15 and 17 under 35 U.S.C. § 102(b) as anticipated by Ishikawa, in paragraphs 18-20 on pages 7-8 of the Office Action claims 4 and 7 were rejected under 35 U.S.C. § 103(a) over Ishikawa in view of Morisada and in paragraphs 21-25 on pages 8-10 of the Office Action, claims 11 and 16 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ishikawa in view of Shiell et al., for substantially the same reasons as in the November 18, 2002 Office Action. The Response to Arguments (paragraphs 26-38) on pages 10-13 of the Office Action, essentially asserted that the claim language is broad enough to read on the different way that Ishakawa discloses execution of branch instructions. Specifically, the claims as previously presented were apparently interpreted as reciting "using mode information to determine which bits in the register constitute the address" (last 2 lines of paragraph 28). Similarly, in paragraph 29, the Examiner asserted that claim 1 "states that the information is used not how the branch instruction is executed" (emphasis in original) and in paragraph 31 on page 11 of the Office Action, the Examiner asserted that "the claim language has not excluded the preexecution cycle ..."

To prevent the claims from being interpreted as indicated in the Response to Arguments, claims 1, 9, 10, 12-15 and 17 have been amended to recite the use of "an instruction fetch pipeline and an instruction execution pipeline and performing an instruction fetch and an instruction execution by way of an out-of-order system" (e.g., claim 1, lines 1-3), as described at 9, lines 9-22 and page 11, lines 13-14. In addition, these claims have been amended to recite that the combination of (address) mode information of a fetched instruction and an instruction address of the fetched instruction is stored "after an instruction fetch request is issued in the instruction fetch pipeline and before the fetched instruction is decoded in a decoding cycle of the

instruction execution pipeline" (e.g., claim 1, lines 5-7), as described at page 11, line 21 to page 12, line 3. Finally, these claims have been amended to recite

> controlling an instruction process of each instruction based on the mode information that has been stored, after the fetched instruction is decoded in the decoding cycle, ... using the mode information that has been stored as mode information of a branch destination of the branch instruction if the fetched instruction is the branch instruction and is not accompanied by a mode change

(e.g., claim 10, lines 9-13), as described at page 20, line 24 to page 21, line 23. Furthermore, claims 11 and 16 have been amended to recite

> a first port of the instruction fetch ports, performing an instruction pre-fetch of a branch destination of a branch instruction based on mode information corresponding to a second port of the instruction fetch ports, and continuing an instruction fetch based on the mode information corresponding to the second port if a branch is performed according to the branch instruction

(e.g., claim 11, lines 9-13), as described at page 24, lines 1-24 and page 26, line 8 to page 27, line 9.

> On the other hand, Ishikawa discloses that
>
> > [a]n address mode bit of a current PSW is set in an address mode bit register 4. When a BSM instruction or a BASSM instruction is loaded into the instruction register 2 and an operation code of the instruction is decoded by a decoder 5, the content of the address mode bit register 4 is set into the bit 0 position of the general purpose register designated by the R1 field of the instruction

(column 3, lines 27-35). Thus, the system taught by Ishikawa has to decode an instruction to determine whether the instruction loaded into instruction register 2 is a BSM instruction or a BASSM instruction. Therefore, the address mode bit is determined after the instruction is decoded. Accordingly, Ishikawa cannot store the combination of address mode information and an instruction address of an instruction before the instruction is decoded, or the pre-fetch as now recited in the claims. Nothing has been cited or found in either Morisada or Shiell et al. suggesting modification of Ishikawa to meet the newly recited limitations. Therefore, it is submitted that claims 1-17 patentably distinguish over any combination of Ishikawa, Morisada and Shiell et al.

**Summary**

It is submitted that the cited references, taken individually or in combination, do not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-17

are in a condition suitable for allowance. Entry of this Amendment, reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 9/9/03

By: _Richard A. Gollhofer_
Richard A. Gollhofer
Registration No. 31,106

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

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STAAS & HALSEY
By: _Richard A. Gollhofer_
Date _9/9/03_